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ABSTRACT OF THE INVENTION

The present invention relates to gate stack structure that is fabricated by a process for selectively plasma etching a structure upon a semiconductor substrate to form a designated topographical structure thereon utilizing an undoped silicon dioxide layer as an etch stop. In one embodiment, a substantially undoped silicon dioxide layer is formed upon a layer of semiconductor material. A doped silicon dioxide layer is then formed upon said undoped silicon dioxide layer. The doped silicon dioxide layer is etched to create the topographical structure. The etch has a material removal rate that is at least 10 times higher for doped silicon dioxide than for undoped silicon dioxide or the semiconductor material. One application of the inventive process includes selectively plasma etching a multilayer structure to form a self-aligned contact between adjacent gate stacks and a novel gate structure resulting therefrom. In the application, a multilayer structure is first formed comprising layers of silicon, gate oxide, polysilicon, and tungsten silicide. An undoped silicon dioxide layer is formed over the multilayer structure. After patterning and etching, the multilayer structure to form gate stacks therefrom, a layer silicon nitride is deposited and is etched to create spacers on the gate stacks that are generally perpendicular to the silicon layer. Doped silicon dioxide is then deposited over the gate stacks and corresponding spacers. A photoresist layer is utilized to expose selective portions of silicon dioxide layer above the contacts on the silicon layer that are to be exposed by etching down through the doped silicon dioxide layer. The doped silicon dioxide is then selectively etched using an anisotropical plasma etch that utilizes a carbon fluorine etch. The novel gate stack structure comprising an undoped silicon dioxide cap is capable of resisting a carbon fluorine etch.

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